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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,572	03/29/2004	James F. Detry	H0002921DIV1 (1016.115210)	2070
128	7590	07/20/2005	EXAMINER	
HONEYWELL INTERNATIONAL INC. 101 COLUMBIA ROAD P O BOX 2245 MORRISTOWN, NJ 07962-2245			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	
DATE MAILED: 07/20/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/811,572	<b>Applicant(s)</b> DETRY ET AL.	
	<b>Examiner</b> James M. Mitchell	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19, 30 and 32-35 is/are pending in the application.
- 4a) Of the above claim(s) 5-8 and 10-13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 9, 14, 16-19, 30, 32, 33 and 35 is/are rejected.
- 7) ☒ Claim(s) 15 and 34 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to the election filed April 19, 2005.

#### ***Election/Restrictions***

2. Claims 5-8, 10-13, withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Applicant's election without traverse of Species I in the reply filed on April 19, 2005 is acknowledged.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 9 and 16, 17, 30-33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaouen et al. (U.S. 6,081,030).
5. Jaouen (Fig. 3, 4) discloses:  
(cl. 1, 30, 32) a method of attaching two portions of wafers, the method comprising:  
providing a first (3) and second wafer (2) having a first (i.e. top portion) and second (i.e. bottom portion) side, creating at least one pit (14) into the first side of the second wafer to define a pillar (i.e. protrusion/ surface area next to item 10); adapting the pillar (104, 106) to conduct an electric signal; providing a contact pad (70) on a first side of the first

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wafer; aligning the first and the second wafer such that the pillar corresponds to the contact pad (Fig. 6); attaching the first wafer to the second wafer;

(cl. 2, 3) providing an inductor (15, 16) that is an electronic component on the second wafer;

(cl.4) wherein the inductor is provided on the first side of the second wafer (Fig. 2);

(cl. 9) and a chip includes a transistor(i.e. "integrated circuit"; Col. 1< lines 5-16)

(cl. 17, 18) with sides slanted;

(cont. cl. 30) and an electronic device having first and second leads (Fig. 3);

(cl. 16, 33) applying metallization (15,16) to the first side area of defining inductive elements, and providing electrical connection (i.e. 10) to leads and first regions ;

(cont. cl. 32) with pad portion on portions of wafer (i.e. portion of 7b expose on top surface of 11);

(cl. 35) applying a dielectric layer (17) over the metallization.

6. Claims 1-4, 9 and 16-18 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Delgado et al. (U.S. 5,825,092).

7. Delgado (Fig. 4-6, 13, 14) discloses:

(cl.1, 30) a method of attaching two wafers, the method comprising: providing a first (82) and second wafer (84) having a first (i.e. top portion) and second (i.e. bottom portion) side, creating at least one pit (96) into the first side of the second wafer to define a pillar (i.e. protrusion under item, 106; Fig. 4); adapting the pillar (104, 106) to conduct an

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electric signal; providing a contact pad (88) on a first side of the first wafer; aligning the first and the second wafer such that the pillar corresponds to the contact pad (Fig. 6); attaching the first wafer to the second wafer;

(cl. 2, 3) providing an inductor (102) that is an electronic component on the second wafer;

(cl.4) wherein the inductor is provided on the first side of the second wafer (Fig. 4);

(cl. 9) and a chip includes a transistor(i.e. "integrated circuit" Title");

(cl. 16) wherein the step of adapting the pillar to conductor includes depositing (Col. 3, Lines 12-13) a conductive material on the pillar;

(cl. 17) providing a slanted side (not labeled side of cavity; Fig. 4) on the pillar, the slanted side being adapted for receiving a deposited conductive material;

(cl. 18) the step of attaching the first and second wafers includes creating a sealed chamber between the first wafer and the second wafer (Col. 1, Lines 7-14); Col. 2, Lines 51-53);

(cont. cl. 30) adapting a second pillar to conduct an electrical signal.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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9. Claims 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaouen (U.S. 6,081,030) in combination with Sakamoto (U.S. 2002/0041021).
10. Jaouen discloses the elements stated in paragraph 5 of this office action, and further discloses a conductive bump (10) forming a seal with first and second wafer portions, but does not disclose the use of solder.
11. Sakamoto teaches solder balls (Par. 0124).
12. It would have been obvious to one of ordinary skill in the art to form the ball of Jaouen of solder in order to form ball as required by Jaouen (10)
13. Furthermore, it would have been obvious to one of ordinary skill in the art to form the ball of solder, since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (CCPA 1960).

#### ***Allowable Subject Matter***

14. Claims 15 and 34 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
15. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or make obvious adapting pillars to conduct an electric signal by doping the pillar, or removing portions of wafer to define pillar and forming metallization over the pillar defining inductive element including placing a via

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from the first side to the second side of the wafer including all the limitations of the independent claim.

### ***Conclusion***

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses in: Johnson (U.S. 2002/0057173) discloses the use of forming metallization on a pillar to form an inductor; Salatino (U.S. 5,915,168) the use of removing material from wafer to form pillars.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

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Jmm  
July 11, 2005

A large, stylized handwritten signature in black ink is written over the text "Jmm July 11, 2005". The signature consists of several loops and vertical strokes, with the first part resembling a large "J" or "G".